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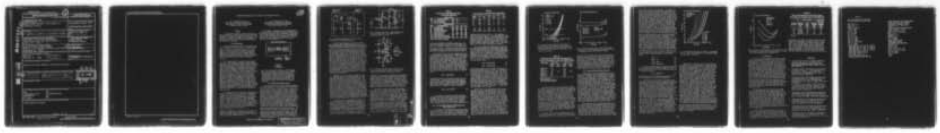

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COMPUTER-AIDED ANALYSIS OF RFI EFFECTS IN INTEGRATED CIRCUITS*

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Summary

A computer-aided analysis procedure based upon a modified Ebers-Moll transistor model is used to predict RFI effects in bipolar integrated circuits (IC's). The procedure is applied to a digital IC to determine the RF power levels that cause several EM susceptibility thresholds to be exceeded.

I. Introduction

The modified Ebers-Moll model for a bipolar junction transistor has been developed for predicting RFI effects in bipolar integrated circuits.[1-3] In this paper it will be shown that the modified Ebers-Moll model can be used with electronic circuit analysis programs such as SPICE (Simulation Program with Integrated Circuit Emphasis) to provide useful information about RFI effects in digital bipolar integrated circuits.[4]

The basic situation of interest is illustrated in Fig. 1. Electromagnetic Radiation (EMR) incident upon a system outer enclosure (skin) is coupled through apertures in the skin to the system interior. The interior EM fields induce RF voltages on the system cables. The RF voltages are conducted to semiconductor devices such as integrated circuits (IC's) located inside electronic equipment. The RF voltages can cause RFI effects in IC's. The example discussed in this paper is illustrated in Fig. 2. The RF voltage induced on a system cable is modeled by the Thevenin equivalent voltage source VGEN with impedance RGEN. The bipolar IC is a 7400 NAND gate (a widely used TTL device). The specific case simulated is the one in which both NAND gate input voltages are high and the NAND gate output voltage is low in the absence of RF injection. The RF is injected into the output terminal because previous experimental and analytical investigations have demonstrated that this case exhibits EM susceptibility effects at lower RF power levels than other cases.[5-7]

Two examples have been selected to illustrate how computer-aided analysis can yield useful information on RFI effects in integrated circuits. In the first example three types of 7400 NAND gates are simulated using the computer program SPICE. These NAND gates are the standard 7400 series, the high speed 74H00 series, and the low power 74L00 series. In the second example a worst case analysis procedure is described which is quite straight-forward. The procedure is used to perform worst case analyses for an RF perturbed 7400 NAND gate when the Thevenin equivalent RF source impedance RGEN is not known apriori.

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This paper is organized in the following manner. In the next section the SPICE simulation procedure using the modified Ebers-Moll model is described. In Section III the SPICE simulation results for the 7400 NAND gate type variation investigation are presented. In Section IV the worst case analysis procedure is described. Section V is the conclusion.

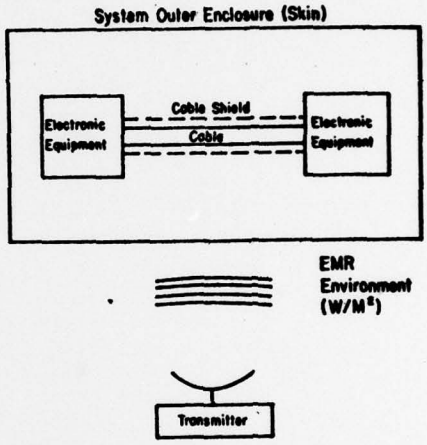

Fig. 1 Basic situation of interest. EMR incident upon the system outer enclosure (skin) is coupled through skin apertures to the system interior. The internal EM fields induce RF voltages on the system cables. These RF voltages are conducted to semiconductor devices such as integrated circuits located inside electronic equipment. The RF voltages can cause RFI effects in integrated circuits.

II. SPICE Simulation Procedure

The electronic circuit analysis program SPICE was developed specifically for analyzing IC's and has been used to predict normal IC operation quite successfully.[4] The phrase "normal IC operation" is used to denote IC operation in an ideal environment in which no RFI signals are present. Unfortunately such ideal environments do not exist everywhere, and IC's must often be operated in environments where strong RFI signals exist. The simulation program SPICE can also be used to predict the effects of RFI upon IC operation using the procedures described in this section. An important point is that no change in an existing SPICE program code is necessary. Standard SPICE models can be used for all IC components not affected by RFI. The transistors into which RF is injected are modeled using the modified Ebers-Moll model described in the previous paper.[1] The modified Ebers-Moll model is implemented by using the external model function available in SPICE.[4] The main steps in the procedure used will be described for the 7400 NAND gate. Similar procedures can be applied to other cases where RF is injected into the terminals of a small-scale bipolar IC.

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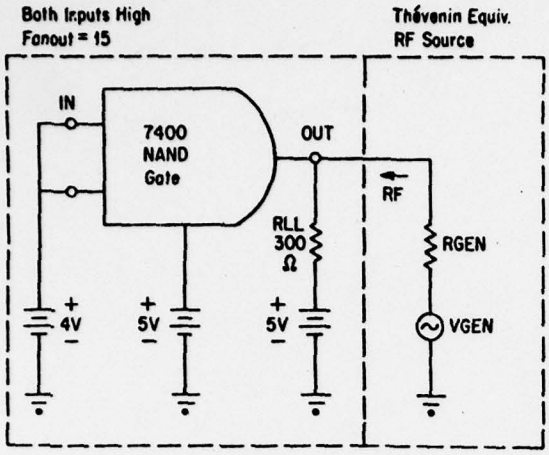

Fig. 2 Schematic illustrating RF signals being coupled into 7400 NAND gate output.

The 7400 bipolar NAND gate was the IC selected for the initial SPICE simulations because it is a widely used digital IC and because its EM susceptibility properties have been extensively measured and reported upon.[5-7] The results of these previous investigations have indicated that 7400 NAND gate operation can be affected significantly by RF injected into several of its terminals. However, the most susceptible case is the one illustrated in Fig. 2 in which RF is injected into the output terminal when the normal output voltage VOUT is low (VOUT < 0.4 V). The output voltage is low when both input voltages VIN are high (VIN > 2.0 V). When both 7400 NAND gate input terminals are high, the RF injected into the output terminal can cause the output voltage to change from its normal low value (VOUT < 0.4 V) to an RF induced higher value (VOUT > 0.8 V). This is the situation that has been simulated using the computer program SPICE. It should also be noted that most members of the 74XX TTL family have essentially identical output circuitry and that the results obtained for the 7400 NAND gate should also be applicable to other 74XX IC's.

Shown in Fig. 3 is a circuit schematic diagram of a 7400 NAND gate with external connections. The 7400 NAND gate includes four resistors (R1-R4), four transistors (T1-T4), and three diodes (D1-D3). The dual emitter transistor T1 will be modeled by a single emitter transistor, and the diodes D1 and D2 will be modeled as a single diode DIN. Previous analyses have shown that when RF is injected into the 7400 NAND gate output (as shown in Fig. 2) that the RF interference can be accounted for by assuming that all the incident RF power is absorbed in the output transistor T4. Thus in this paper only the case in which the transistor T4 absorbs all the incident RF power is considered. One result is that the standard component models available in SPICE can be used for all 7400 NAND gate components except the transistor T4. The transistor T4 is modeled using the modified Ebers-Moll model shown in Fig. 4.

The first step in the simulation procedure involves determining the 7400 NAND gate parameters required to simulate its normal (no RFI) operation. Values for the resistors R1-R4 are available on manufacturer's data sheets but values for the diode and transistor parameters are not. If no information on the 7400 NAND gate diode and transistor parameters were available, the SPICE default or typical values would have been used.[4] Fortunately, at least one source of information on 7400 NAND gate parameters is

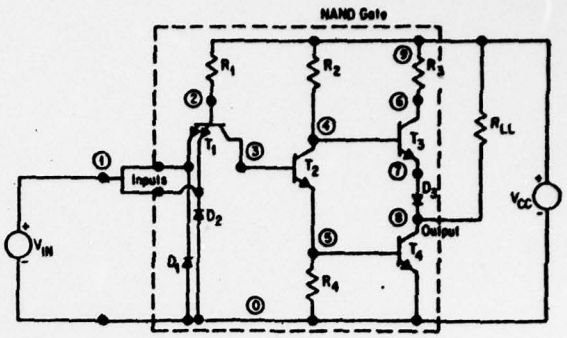

Fig. 3 Schematic diagram of a 7400 NAND gate with external connections. Node numbers used in SPICE simulations are shown.

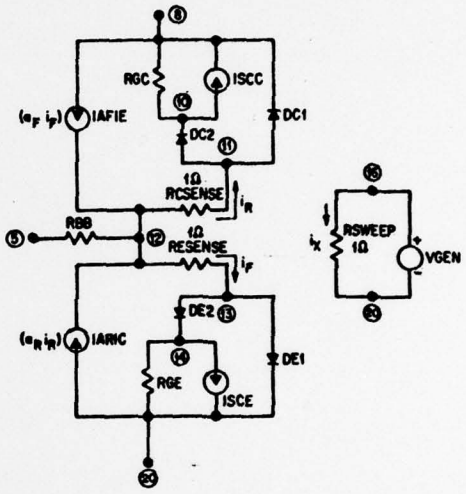

Fig. 4 Modified Ebers-Moll model in an external model configuration for SPICE simulations. Node numbers used in SPICE simulations are shown.

available.[8] Although this information is presented in a format for use with the electronic circuit analysis program SCEPTRE, it can be readily converted to the format used in the program SPICE. The resulting SPICE parameter values are given in Table I for the diodes and transistors in the 7400 NAND gate. These parameter values are entered as data for a SPICE simulation. (See Table AI in the Appendix for an example of data for a SPICE simulation of an RF perturbed 7400 NAND gate).

Also given in Table I for the 7400 NAND gate transistors are the modified Ebers-Moll model parameter values which do not depend upon the RF power. The transistor T4 into which all the RF power is assumed injected is modeled using the modified Ebers-Moll model shown in Fig. 4. The modified Ebers-Moll model is incorporated in the SPICE data cards as an external model as shown in Table AI in the Appendix. (For a detailed description on using external models in the program SPICE, see the SPICE user's manual).[4] To implement the current-dependent current sources IAFIE and IARIC in the modified Ebers-Moll model, 1 Ω current sensing resistors RESENSE and RCSENSE are placed in the emitter and collector circuit as shown in Fig. 4. The current sources IAFIE ($\alpha_F I_F$) and IARIC ($\alpha_R I_R$) are made to depend upon the voltage drops V12 - V13 and V12 - V11 across

TABLE I
Diode and Transistor Parameter Values for the 7400 NAND Gate

Diode Parameters

Name	Parameter Description	D1N	D3
RS	Ohmic Resistance (Ω)	60	30
IS	Saturation Current (pA)	100	5

Transistor Parameters

Name	Parameter Description	T1	T2	T3	T4
BF	Forward Beta (βF)	.316	19.8	17.2	21.7
BR	Reverse Beta (βR)	.0024	.060	.082	.106
RB	Base Ohmic Resistance (Ω)	68	75	70	80
IS	Saturation Current (pA)	.5	3	8	20
AF*	Forward Alpha (αF)	.24	.952	.945	.956
AR*	Reverse Alpha (αR)	.0024	.057	.076	.0956
IES*	Emitter Diode Sat. Current (pA)	2	3	8	20
ICS*	Collector Diode Sat. Current (pA)	200	50	100	200

*Parameter used in modified Ebers-Moll Model.

the resistors RESENSE and RCSENSE respectively. The result is that IAFIE = AF (V12 - V13) and IARIC = AR• (V12 - V11) where the values for AF (α_F) and AR (α_R) are given in Table I. The diodes DE1 and DE2 both have the saturation current IES and the diodes DC1 and DC2 both have the saturation current ICS given in Table I.

Also shown in Fig. 4 is a dc voltage source with a voltage equal to the amplitude of VGEN of the Thevenin equivalent RF source shown in Fig. 2. The dc voltage source controls the voltage V16-V20 which controls the RF induced dc current generators ISCE and ISCC. The exact relationship between ISCE and ISCC and VGEN must be determined by the user. Two different procedures for relating ISCE and ISCC to VGEN will be described in the next two sections. (Similar statements apply to the RF induced resistors RGE and RGC.) By causing VGEN to vary over an appropriate range of values, the values for ISCE and ISCC are made to vary also. To determine the appropriate range of values for VGEN the relationship

$$PINC = VGEN^2/8RGEN \qquad (1)$$

is used where PINC is the RF power incident upon the 7400 NAND gate. The value for PINC is assumed to be equal to the maximum available power from a Thevenin equivalent RF source of amplitude VGEN and impedance RGEN. This may be viewed as a worst case assumption. When RGEN is 50 Ω, Equation (1) may be written as

$$VGEN = (400\ PINC)^{0.5} \qquad (2)$$

In the next two sections the SPICE simulation procedure described in this section will be applied to determine the relative EM susceptibility of various 7400 NAND gate types (Section III) and to perform a worst case analysis when the RF Thevenin equivalent source impedance RGEN is not known apriori (Section IV).

III. EM Susceptibility of the NAND Gate Types 7400, 74H00, 74L00

Three types of 7400 NAND gates have been investigated to determine their relative susceptibility to RFI. These are the normal 7400 series, the high speed 74H00 series, and the low power 74L00 series. These three NAND gate series use different values for the internal

TABLE II
Resistor Values for 7400 NAND Gate Type Variations

Resistor (kΩ)	7400	Fan-out	7400H	Fan-out	7400L	Fan-out
R1	4.38	—	2.80	—	40	—
R2	1.43	—	0.70	—	20	—
R3	0.116	—	0.116	—	0.116	—
R4	1.06	—	1.06	—	12	—
RLL	4.38	1	2.80	1	40	1
RLL	0.30	15	0.28	10	4	10

resistances R1-R4 shown in Fig. 3. The resistance values are given in Table II. The three NAND gate types have the same output stage, but the resistance R1 in the input stage varies. The variation in the value for R1 manifests itself in the value of the resistor RLL required to simulate different fanout values. The values of RLL required to give a low fanout (F = 1) and a high fanout (F = 10 or 15) are also given in Table II.

To use the simulation program SPICE to calculate the effects RF injected into the NAND gate output will have upon NAND gate operation, the procedure described in the previous section is applied. The standard SPICE models are used for all NAND gate components except the transistor T4. The transistor T4 is modeled by the modified Ebers-Moll model. This model contains two RF induced dc current generators ISCE and ISCC which depend upon the value of the Thevenin equivalent RF generator voltage amplitude VGEN:[2]

$$ISCE = (KE/RGE)VGEN \qquad (3)$$

$$ISCC = (KC/RGC)VGEN \qquad (4)$$

The parameter values for KE, KC, RGE, and RGC were determined experimentally at 220 MHz for a 2N2369A NPN transistor which is believed to be similar to the output transistor T4 in the 7400 NAND gates. The values determined are KE = 0.12, KC = 0.72, RGE = 180 Ω, RGC = 190 Ω, KE/RGE = 0.067 mυ, and KC/RGC = 3.79 mυ. The ratios (KE/RGE) and (KC/RGC) are effectively transconductances which relate the RF induced dependent current generators ISCE and ISCC to the control voltage VGEN. (See SPICE data given in Table AI in the Appendix). The control voltage VGEN is related to the RF incident power PINC by Eq. (2) when RGEN = 50 Ω. Varying VGEN over the range 0.2 to 20 V corresponds to varying PINC over the range -10 to +30 dBm.

Shown in Fig. 5 are the predicted values of the NAND gate output voltage VOUT plotted versus the RF incident power PINC. The plots shown in Fig. 5 indicate the relative EM susceptibility of the three NAND gate types with low (F = 1) and igh (F = 10 or 15) fanouts. When no RF power is applied, the output voltage VOUT is low (approximately 0.1 V). As the RF power increases, the VOUT values increase. The selection of EM susceptibility threshold levels at which an RF induced malfunction is said to occur is one of the important decisions that an EMC engineer must make. An EM susceptibility threshold level of VOUT = 0.8 V corresponds to the upper allowed voltage value that a subsequent stage is guaranteed to recognize as a low state input. The value VOUT = 2.0 V corresponds to a VOUT value certain to be recognized as a high state (rather than a low state) by a subsequent NAND gate input. The values of RF power which cause these two EM threshold levels to be exceeded are given in Table III.

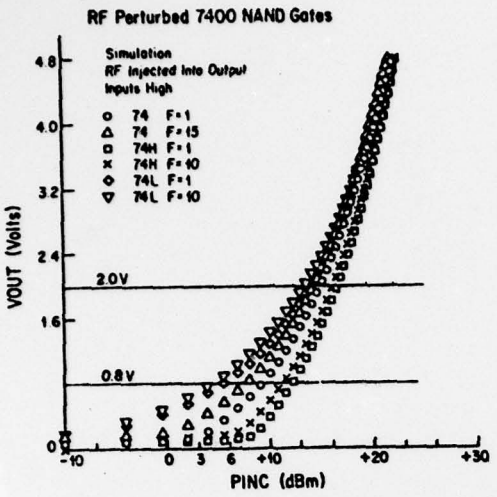

Fig. 5 SPICE simulation values of the outnut voltage VOUT vs. the incident RF power PINC for three 7400 NAND gate types with different fanouts. EM susceptibility thresholds at VOUT equal to 0.8 and 2.0 V are shown.

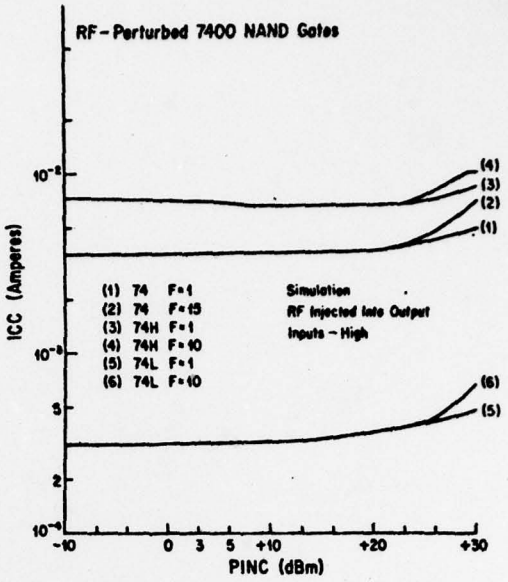

Fig. 6 SPICE simulation values of the power supply current ICC vs. the incident RF power PINC for three 7400 NAND gate types with different fanouts.

TABLE III

Values of RF Power Which Cause EM Susceptibility Criteria To Be Exceeded for Three 7400 NAND Gate Types

Type of Gate	VOUT = 0.8 V		VOUT = 2.0 V	
	SPICE[a] P_I(dBm)	Exp.[b] P_A(dBm)	SPICE[a] P_I(dBm)	Exp.[b] P_A(dBm)
7400L (F=10)	4.4		13.4	
7400L (F=1)	5.4		14.0	
7400 (F=15)	7.6	6.0	14.5	14.5
7400 (F=1)	9.0		14.8	
7400H (F=10)	11.2		16.0	
7400H (F=1)	12.2		16.5	

[a] Values of incident RF power.

[b] Values of absorbed RF power. - See Ref (6). Values of incident RF power would be higher.

The SPICE simulation results presented in Table III indicate that the low power 74L00 series NAND gates are the most susceptible to RFI and that the high speed 74H00 series NAND gates are the least susceptible to RFI. For each NAND gate type the fanout value has a small effect (less than 2 dB) upon the RF power required to cause the two EM susceptibility threshold levels to be exceeded. Also given in Table III are experimental values for the absorbed RF power required to cause the 7400 NAND gate series output voltage VOUT to exceed the two EM susceptibility threshold levels.[6] These experimental values are in good agreement with the values predicted by the SPICE simulations. This agreement indicates that the modified Ebers-Moll model can be used in an electronic circuit analysis program such as SPICE to predict RFI effects in digital bipolar IC's quite well.

Plotted in Fig. 6 are the predicted values of the NAND gate power supply current ICC versus the RF incident power PINC. It is observed that for RF power levels less than +20 dBm that little change occurs in the power supply current ICC. However, by referring to Figure 5 it is observed that for an RF incident power level equal to +20 dBm that the NAND gate output voltage VOUT exceeds 3.5 V for all NAND gate types. Thus it is believed that in almost all applications the increase in 7400 NAND gate output voltage VOUT will cause circuit malfunctions at lower values of PINC (+4 to + 12 dBm) than the values of PINC(>+ 20 dBm) required to cause increases in the power supply current ICC.

IV. A Worst Case Simulation Procedure

In the previous section the impedance of the RF generator connected to the 7400 NAND gate was assumed to be 50 Ω. The main reason for making this assumption was to permit a comparison of SPICE simulation results to the available experimental results which were obtained by injecting RF power into a 7400 NAND gate from an RF generator with 50 Ω internal impedance. In an actual RFI environment (as opposed to a laboratory environment) EM fields incident upon an electronic system will be coupled through the electronic system enclosure to the interior. (See Fig. 1.) The EM fields inside the electronic system enclosure will induce RF voltages and currents on the wires connected to IC's. The RF voltages induced on the wires can be represented by a Thevenin equivalent voltage source of amplitude VGEN and impedance RGEN. In general the impedance RGEN will not be 50 Ω but can be expected to lie in the range 5 to 5000 Ω. The objective of this section is to describe a generalized worst case analysis procedure which can be used in the situation in which the RF Thevenin equivalent source impedance RGEN is not known apriori.

The generalized worst case analysis procedure to be described uses the modified Ebers-Moll model shown in Fig. 4. Recall that this model contains two dc current generators ISCE and ISCC and two resistors which depend upon the RF power incident upon the transistor being modeled. The method used to assign values to these four parameters differs from that used in the previous section. The new method used to assign values to ISCE, ISCC, RGE, and RGC is quite general and appears

well-suited for worst case analyses. As discussed in the previous paper the modified Ebers-Moll model shown in Fig. 4 for a bipolar junction transistor (BJT) resembles the standard Ebers-Moll model with the standard collector-base diode DC1 shunted by the RF induced components DC2, RGC, and ISCC and with the standard emitter base diode DE1 shunted by the RF induced components DE2 RGE, and ISCE. The diode DC2 is identical to the diode DC1, and the diode DE2 is identical to the diode DE1. The specific case being simulated is a 7400 NAND gate with RF power injected into its output terminal which is connected internally to the collector of the transistor T4 as shown in Fig. 3. For RF power injected into the collector of a BJT with the specified external (to the transistor) bias and load conditions, the worst case simulation results are obtained when all the RF power is assumed to go into the collector-base junction with no RF power going into the emitter-base junction.[6] Since the emitter-base junction is assumed to absorb zero RF power, the values ISCE = 0 and RGE = ∞ are assigned to the emitter base junction parameters. (The SPICE data cards for these circuit elements are omitted.) Since the collector-base junction is assumed to absorb all the RF power, the values assigned to the collector-base junction parameters are ISCC = VGEN/RGEN and RGC = RGEN. As discussed in the previous paper this assignment over-estimates the dc rectified current produced in a diode connected to an RF source of amplitude VGEN and impedance RGEN.[1] This is the main reason that the procedure being described is called a worst case analysis procedure. These assignments are summarized below:

$$RGE = \infty \tag{5}$$

$$ISCE = 0 \tag{6}$$

$$RGC = RGEN \tag{7}$$

$$ISCC = VGEN/RGEN \tag{8}$$

To relate the RF generator voltage amplitude VGEN to the incident RF power PINC, Equation (1) is used. Particularly useful is the value of VGEN for which PINC = 1 W which is given by

$$VGEN = (8RGEN)^{0.5} \tag{9}$$

Equations (5) - (9) are used to assign values to the circuit parameters in the SPICE simulations.

As in the previous section the situation being simulated is the one in which both NAND gate inputs are high and the output is low in the absence of injected RF. The value for the resistor RLL is set equal to 300 Ω which corresponds to a fanout F = 15. (The results of the previous section indicate that the higher fanout value leads to EM susceptibility effects at slightly lower RF incident power levels than does a low fanout value such as F = 1.) The first step in the simulation procedure is to assign a value for the impedance RGEN of the Thevenin equivalent RF source. The current generator ISCC is calculated using Eq. (8). Next the voltage generator amplitude VGEN is swept from 0.00 to $(8RGEN)^{0.5}$ in steps equal to $(8RGEN)^{0.5}/100$. Recall from Eq. (9) that the maximum VGEN amplitude corresponds to PINC = 1 W. The corresponding values for the RF incident power PINC are calculated using Eq. (1). Values for the NAND gate output voltage VOUT are plotted versus values of PINC for each value of RGEN selected as shown in Fig. 7. Using the SPICE simulation results shown in Fig. 7, the values of the incident power PINC that cause VOUT to equal EM susceptibility threshold levels equal to 0.4, 0.8, and 2.0 V were determined.

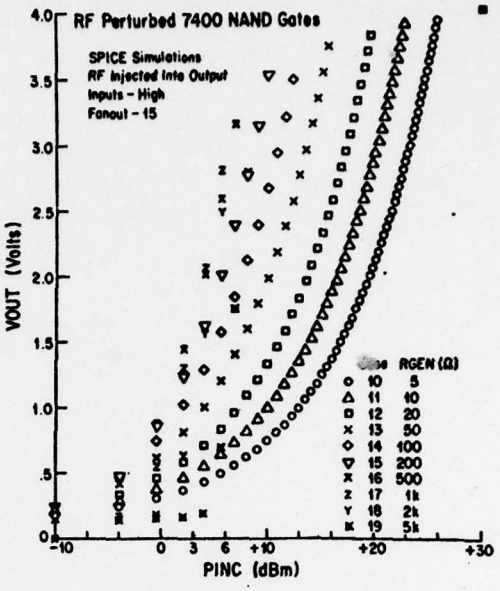

Fig. 7 SPICE simulation values of VOUT for a 7400 NAND gate vs. PINC. The RF Thevenin source impedance RGEN is varied from 5 to 5000 Ω.

Shown in Fig. 8 are the values of PINC required to cause VOUT for a 7400 NAND gate to exceed the three selected EM susceptibility criteria plotted versus the RF generator impedance RGEN. It is observed that for each EM susceptibility threshold level that the PINC vs. RGEN plot has a minimum PINC value. These minimum PINC values are summarized in Table IV along with the corresponding RGEN values. Upon examining the values given in Table IV, it is observed that for the VOUT = 0.8 and VOUT = 2.0 V EM susceptibility threshold levels that the minimum PINC values are lower than the PINC values at RGEN = 50 Ω by 2.5 and 6.0 dB respectively. The SPICE simulation results clearly indicate that the PINC values required to cause VOUT to exceed the higher threshold levels do depend upon the impedance RGEN of the Thevenin equivalent RF source. Experimental results for values of RGEN other than 50 Ω to which the SPICE simulation results might be compared are not available. Nor are such experimental results easily obtained at UHF frequencies where most coaxial transmission line equipment has a 50 Ω characteristic impedance. However, the SPICE simulation results with RGEN = 50 Ω can be compared to experimental results obtained with RGEN = 50 Ω . As shown in Table IV these results agree within 4 dB. The good agreement obtained for the special case RGEN = 50 Ω between simulated and experimental results gives us confidence that the simulation procedures developed are reliable and that these procedures can be extended to the more general case where RGEN is not 50 Ω . The simulation results given in Fig. 8 and Table IV provide a usable estimate of the minimum RF incident power required to cause various EM susceptibility threshold levels to be exceeded.

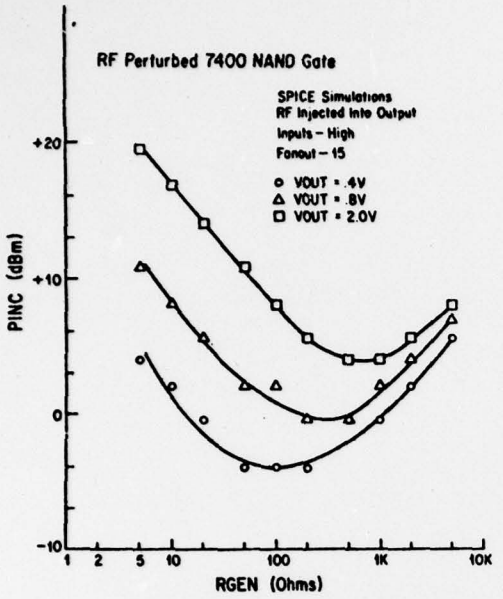

Fig. 8 Values of PINC required to cause VOUT for a 7400 NAND gate to exceed various EM susceptibility criteria vs. the RF Thevenin source impedance RGEN.

V. Conclusion

It has been demonstrated that electronic circuit analysis programs such as SPICE can be used to predict the effects of RFI upon bipolar digital IC's such as 7400 NAND gates. The most important requirement is a good model for the bipolar transistor in which RF is injected. The modified Ebers-Moll model described in the previous paper is such a model. The procedures for using the modified Ebers-Moll model as an external model in the simulation program SPICE were described in Section II. No change in an existing SPICE computer code is required. In subsequent sections these procedures were applied to determine the EM susceptibility of a 7400 NAND gate with both inputs high and the output low (with no RFI present) when RF power was injected into its output since previous investigations had indicated that this was the most susceptible case.[5-7] The simulations reported upon used standard SPICE models for all components in the 7400 NAND gate except for the output transistor. The output transistor into which RF was injected was modeled using the modified Ebers-Moll model.

The EM susceptibility of three types of NAND gates was investigated. Experimentally determined values were used for the RF induced parameters in the modified Ebers-Moll model. The SPICE simulations indicated that the low power 74L00 series NAND gates are the most susceptible and that the high speed 74H00 series NAND gates are the least susceptible. Variations in fanout cause less than a 2 dB variation in the incident RF power required to cause various EM susceptibility threshold levels to be exceeded. To summarize the SPICE simulation results: all three types of the 7400 NAND gates will malfunction in most circuit applications at injected RF power levels in the +6 to +16 dBm range.

A worst case analysis procedure also was described. The procedure described is quite general in that the impedance RGEN of the Thevenin equivalent RF source connected to the IC can be varied in a systematic manner. This procedure is especially useful when the RGEN value is not known apriori. Values for the RF power PINC in the range -4 to +4 dBm caused the three selected EM susceptibility threshold levels to be exceeded. For the special case RGEN = 50 Ω the simulation results and experimental results agreed within 4 dB. (The predicted results are more conservative than the experimental results which is desirable in a worst case analysis.) As stated previously the good agreement obtained for this case makes us confident that the simulation procedures are reliable and useful.

TABLE IV

Values of PINC Required to Cause VOUT to Exceed EM Susceptibility Threshold Levels for 7400 NAND Gates

	SPICE Simulations			Experimental[a] (Worst Case)
Threshold Level for PINC	RGEN Value at Minimum PINC	PINC Minimum Value	PINC Value When RGEN = 50 Ω	PINC Value When RGEN = 50 Ω
V	Ω	dBm	dBm	dBm
0.4	50-200	-4	-4	-3
0.8	200-1000	-0.5	+2	+6
2.0	500-1000	+4	+10	+13

[a] Ref. (7), p.4.

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TABLE AI

DATA CARDS FOR A SPICE SIMULATION
OF AN RF PERTURBED 7400 NAND GATE

```
VCC 9 0 DC 5
VIN 1 0 DC 4.25
VGEN 16 0
*NODE 0 = NODE 20
R1 9 2 4.38K
R2 9 4 1.43K
R3 9 6 0.116K
R4 5 0 1.06K
RL 1 0 .2K
RLL 8 9 9.11K
QT1 3 2 1 MOD1
QT2 4 3 5 MOD2
QT3 6 4 7 MOD3
XT4 8 5 0 16 RF-EBML
DIN 0 1  MOD5
D3  7 8  MOD6
·MODEL MOD1 NPN .316 .0024 68  IS=5E-13
·MODEL MOD2 NPN 19.8 .060  75  IS=3E-12
·MODEL MOD3 NPN 17.2 .082  70  IS=8E-12
·MODEL MOD4 NPN 21.7 .106  80  IS=2E-11
·MODEL MOD5 D RS=60 IS=1E-10
·MODEL MOD6 D RS=30 IS=5E-12
·DC TC VGEN .2 20 .2
*BY CAUSING VGEN TO VARY THE
*CURRENT GENERATORS ISCC AND ISCE
*WHICH DEPEND UPON THE VOLTAGE ACROSS
*RSWEEP ALSO VARY, THIS SIMULATES
*A CHANGE IN INCIDENT RF POWER.
·OUTPUT VOUT 8 0   PLOT DC 0 5
·TEMP 20
* MDAC RF MODIFIED EBERS-MOLL MODEL
·MODEL RF-EBML X 8 5 20 16
IAFIE V 8 12 12 13 0.956
IARIC V 20 12 12 11 0.0956
RBB 5 12 80
RCSENSE 12 11 1
RESENSE 12 13 1
DC1 11 8 MOD7
DE1 13 20 MOD8
·MODEL MOD7 D IS=200P
·MODEL MOD8 D IS=20P
*RF INDUCED TERMS (ELEMENTS)
RSWEEP 16 20 1
RGC 8 10 190
RGE 14 20 180
ISCC V 10 8 16 20 3.79M
ISCE V 14 20 16 20 0.667M
DC2 11 10 MOD7
DE2 13 14 MOD8
·FINIS
·END
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